

IN THE CLAIMS:

1 1. (currently amended) A method of forming a layer of interconnect in
2 an integrated circuit comprising the steps of:
3 depositing a first layer of interlayer dielectric (ILD) on a lower layer of
4 said integrated circuit above a set of lower alignment marks;
5 depositing a first hardmask layer of TaN on said first layer of ILD, said
6 first layer being substantially transparent in a relevant wavelength range in
7 which said hardmask layer has a resistivity greater than about 400 micro
8 Ohm-cm;
9 forming an upper set of alignment marks;
10 patterning said ILD through said hardmask layer to form a set of apertures
11 in said ILD; and
 forming a conductive interconnect in said set of apertures.

1 2. (currently amended) A method of forming a layer of interconnect in
2 an integrated circuit comprising the steps of:
3 depositing a first layer of interlayer dielectric (ILD) on a lower layer of
4 said integrated circuit above a set of lower alignment marks;
5 depositing a first hardmask layer of TaN on said first layer of ILD, said
6 first layer being substantially transparent in a relevant wavelength range;
7 forming an upper set of alignment marks;

. 8 patterning said ILD through said hardmask layer to form a set of apertures
9 in said ILD; and

10 forming a conductive interconnect in said set of apertures;

11 in which said hardmask layer is deposited by sputter deposition of Ta in
12 an ambient containing N₂ and a carrier gas such that (N₂flow)/(N₂ + carrier
13 flow) > 0.5.

1 3. (original) A method according to claim 1, in which said hardmask
2 layer is deposited by chemical vapor deposition by reacting a precursor gas
3 containing Ta in an ambient containing N₂.

1 4. (original) A method according to claim 2, in which said hardmask
2 layer is substantially transparent in said relevant wavelength range.

1 5. (original) A method according to claim 3, in which said hardmask
2 layer is substantially transparent in said relevant wavelength range.

1 6. (original) A method according to claim 2, in which said hardmask
2 layer has a resistivity greater than about 400 micro Ohm-cm.

1 7. (Canceled)

1 8. (original) A method according to claim 2, in which said hardmask
2 layer has a thickness ranging from 5nm to 100nm.

1 9. (original) A method according to claim 3, in which said hardmask
2 layer has a thickness ranging from 5nm to 100nm.

1 10. (original) A method according to claim 2, in which said hardmask
2 layer has a composition of less than 50% Ta.

1 11. (original) A method according to claim 3, in which said hardmask
2 layer has a composition of less than 50% Ta.

1 12. - 22 (canceled)